What is claimed is:

1. An ATM SAR (Asynchronous Transfer Mode Segmentation and Reassembly) module for a xDSL communication service chip, comprising:

a memory control means for generating a control signal for accessing a packet memory;

a generation means for transmitting a CRC32, which is a block to generate 32 bits CRC (Cyclic Redundancy Check) block necessary for the AAL (ATM adaptation Layer)-5 PDU (Protocol Data Unit) and calculating the AAL-5 PDU in a virtual unit;

a generation means for receiving the CRC32 that is a block to check an error of the AAL-5 PDU inputted through the other network;

a CRC10 processing means for transmitting and receiving a CRC10 that processes the OAM (Operation, Administration and Maintenance) cell;

a header manager means for adding or analyzing 4 octets ATM header according to virtual channel setup information of a transmitted the AAL-5 PDU and data types (AAL-5 PDU or OAM cell) to be processed;

an UTOPIA interface means for controlling a standard connection between the ATM SAR and a physical module;

an ATM SAR state management means for controlling whole operations of the ATM SAR; and

a packet memory means for storing data to be received or transmitted through the ATM SAR

2. The ATM SAR module as recited in claim 1, wherein the packet memory means is a dual port memory.

3. The ATM SAR module as recited in claim 2, wherein the packet memory means includes a transmission and reception packet memories.

4. The ATM SAR module as recited in claim 3, wherein the transmission and reception packet memories are memories which are symmetrically assigned according to traffic characteristic of a virtual channel to be set up at the same time.

5. The ATM SAR module as recited in claim 4, wherein the transmission and reception packet memories are dynamically re-assigned according to a virtual channel assignment.